EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	33	703/14.ccls. and @pd>"20071101"	US-PGPUB	OR	OFF	2008/04/07 12:30
L2	1307	cache same test$3 and @ad<"20040301"	US-PGPUB	OR	OFF	2008/04/07 12:40
L3	69	cache near test$3 and @ad<"20040301"	US-PGPUB	OR	OFF	2008/04/07 12:40
L4	43	cache near test$3 and random and @ad<"20040301"	US-PGPUB	OR	OFF	2008/04/07 12:40
L5	73	(cache same test$3 same random) and @ad<"20040301"	US-PGPUB	OR	OFF	2008/04/07 12:50
L6	64	L5 NOT L4	US-PGPUB	OR	OFF	2008/04/07 12:50
L7	10	((cache near design) same test$3) and @ad<"20040301"	US-PGPUB	OR	OFF	2008/04/07 12:57

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L10	0	((cache near design) same verif$7) and random	US-PGPUB	OR	OFF	2008/04/07 14:00

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L12	56	(cache and sequential$2 and random$2 and function$1).clm.	US-PGPUB	OR	OFF	2008/04/07 14:27
L14	14	(cache and buffer$1 and random$2 and verif$7).clm.	US-PGPUB	OR	OFF	2008/04/07 14:35

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Protocol **verification as a hardware design** aid - all 14 versions »
DL Dill, AJ Drexler, AJ Hu, CH Yang - Computer Design' VLSI in Computers and Processors, 1992. ..., 1992 - ieeexplore.ieee.org
... more bugs in the original **design** are uncovered ... The **verification** process then enters a tight loop ... 3.1 **Cache** coherence protocol Directory-based **cache** coherence is ...
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DA Patterson, JL Hennessy - 1990 - portal.acm.org
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JR Burch, DL Dill - ... 6th International Conference on Computer Aided **Verification**, 1994 - Springer
... with these com- plications seems to be justified since the **cache** hit ratio is ... In G. Birtwistle, editor, Proceedings of the 1988 **Design Verification** Conference. ...
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Verification of the Futurebus+ **cache** coherence protocol - all 7 versions »
EM Clarke, O Grumberg, H Hiraishi, S Jha, DE Long, ... - Formal Methods in System **Design**, 1995 - Springer
... Our model for the **cache** coherence protocol consists ... to reduce the complexity of **verification** (by hiding details) and to cover allowed **design** choices (indicated ...
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Verifying a Multiprocessor **Cache** Controller Using Random Test Generation - all 8 versions »
DA Wood, GA Gibson, RH Katz - IEEE **Design** & Test, 1990 - portal.acm.org
... DOI Bookmark: 10.1109/54.57906. ABSTRACT The **design verification** of the **cache** controller for SPUR, a shared-memory multiprocessor, is reported. ...

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Constraint solving for test case generation: a technique forhigh-level **design verification** - all 2 versions »
AK Chandra, VS Iyengar - Computer **Design**: VLSI in Computers and Processors, 1992. ..., 1992 - ieeexplore.ieee.org
... **Random** test patterns have been extensively used for **design verification** of CPU pipelines, arithmetic units, controllers, **cache** memories, etc. ...
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[PDF] **Verification** of the IBM RISC System16000 by a dynamic biased pseudo-**random** test program generator - all 5 versions »
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... HDL simulation with **random**, serf checking vector ... by a discussion of effective **design verification** techniques used ... UO, and may also support **cache**-coherence and ...
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Design verification of the S3. mp **cache**-coherent shared-memorysystem - all 7 versions »
F Pong, M Browne, A Nowatzyk, M Dubois - Computers, IEEE Transactions on, 1998 - ieeexplore.ieee.org
... applied to validate the memory system **design** of the ... that development and validation of **cache** proto- cols ... greatly benefit from state-based **verification** methods. ...
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... by a discussion of effective **design verification** techniques used ... implements a number
of **design** features tomaintain ... a complete set of duplicate **cache** tags which ...
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... In order to manage the size of the prototype **design** effort, a commercial ... interfaces to a 256 Kbyte second-level write-back **cache** through a read **buffer** and a ...
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